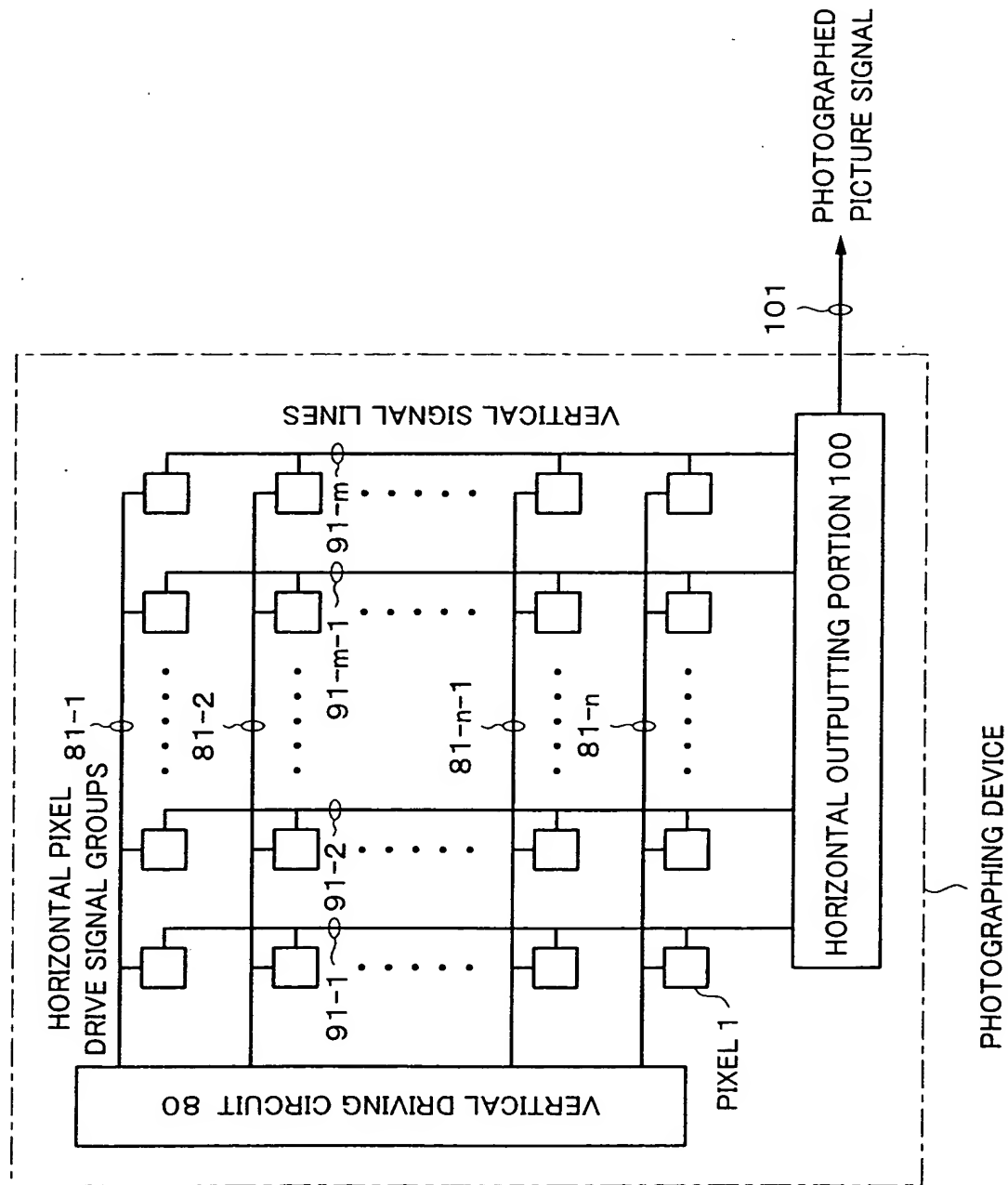


Fig. 1



The diagram illustrates the internal structure of a pixel circuit, labeled "PIXEL 1". The signal flow is as follows:

- Light Input (11):** Represented by a wavy arrow, it enters the **LIGHT RECEIVING PORTION (10)**.
- First Amplification (20):** The signal from the light receiving portion is sent to the **FIRST AMPLIFYING PORTION (20)**.
- Second Amplification (30):** The output of the first amplifying portion is sent to the **SECOND AMPLIFYING PORTION (30)**.
- Storage (40-1 to 40-k):** The output of the second amplifying portion is distributed to a series of **STORING PORTIONS** (40-1, 40-2, ..., 40-k).
- Calculation and Biasing (50, 55):** The outputs from the storing portions are sent to the **LOAD PORTION AND CALCULATING PORTION (50)**. This portion also receives a **BIAS PORTION (55)** signal.
- Output (60):** The output of the load and calculating portion is sent to the **OUTPUTTING PORTION (60)**.
- External Connections:** The circuit is connected to external nodes 11, 21, 31, 41, 51, 61, and 70.

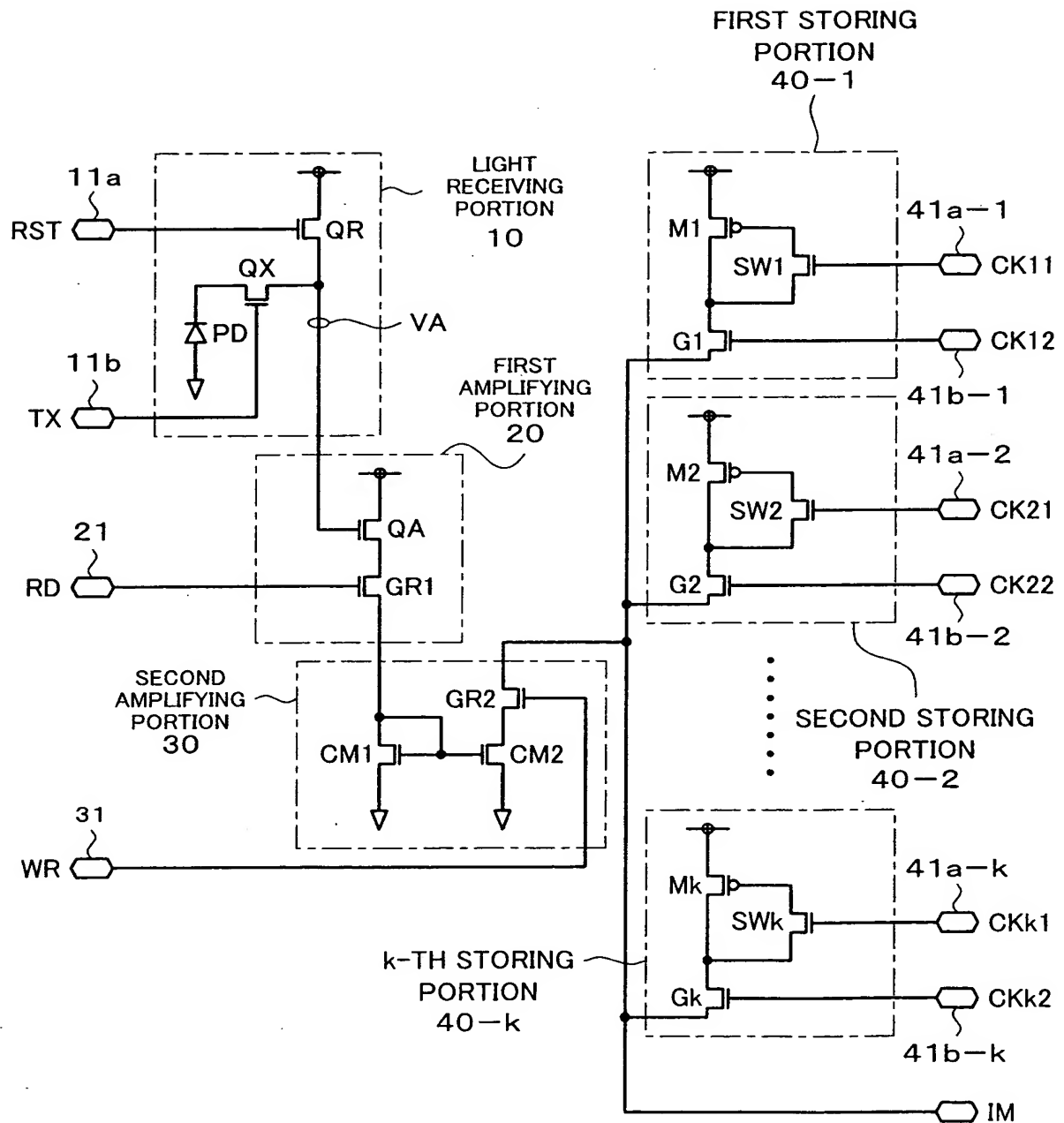
Fig. 3

Fig. 4

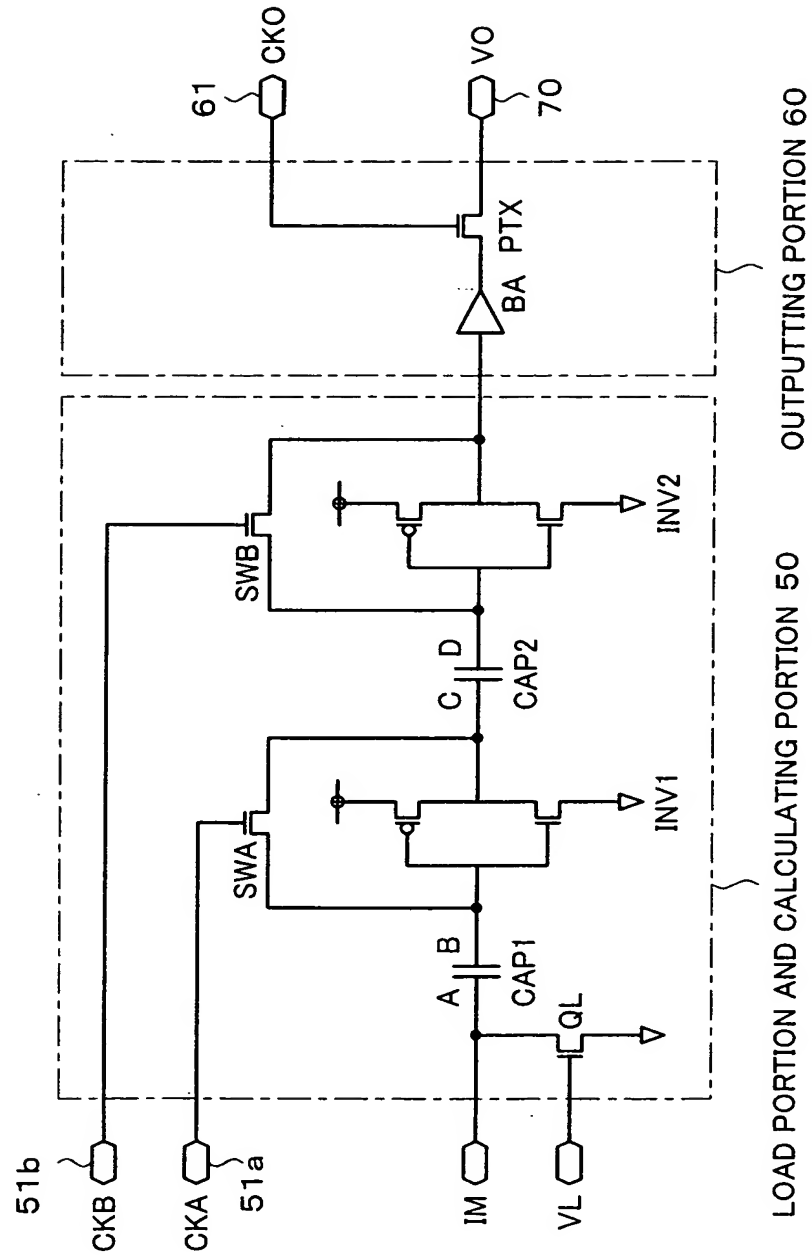
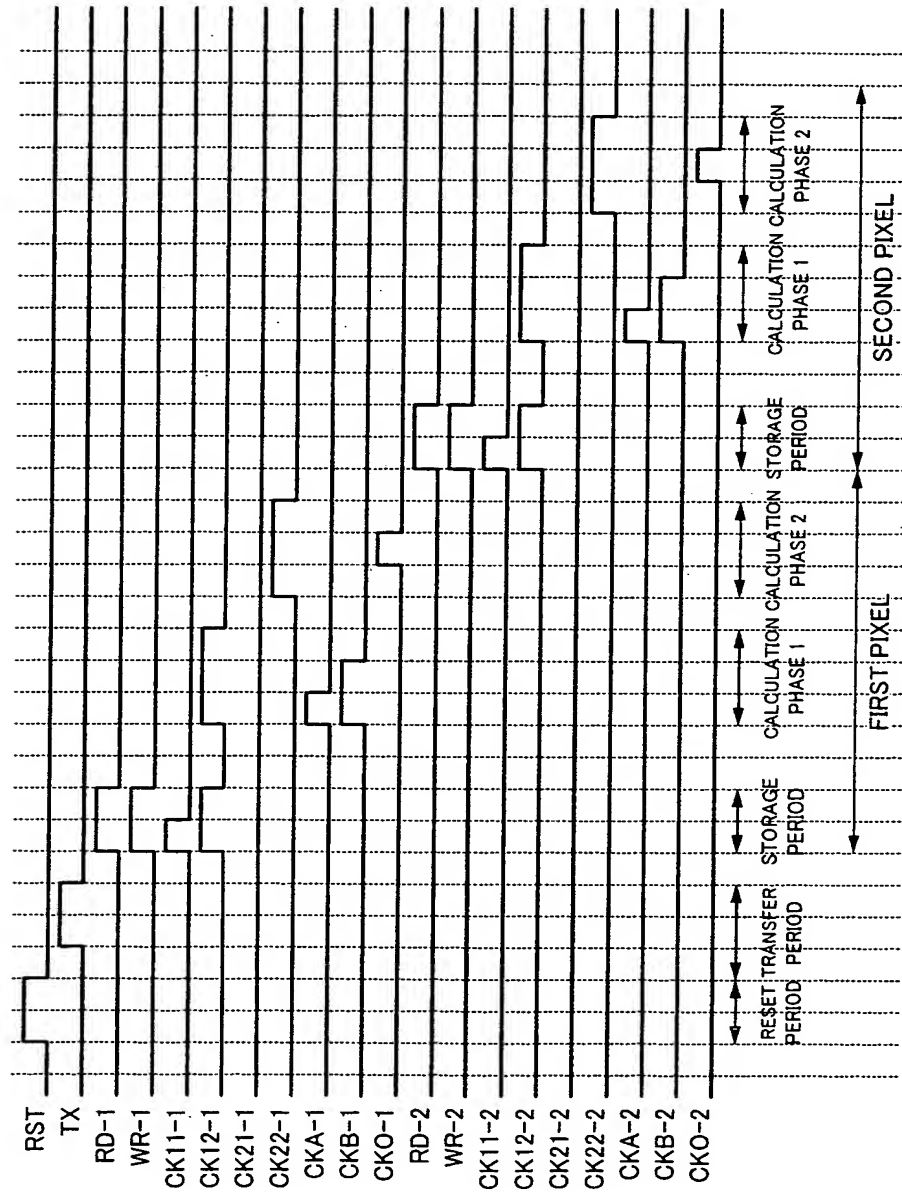


Fig. 5



205050-256000T

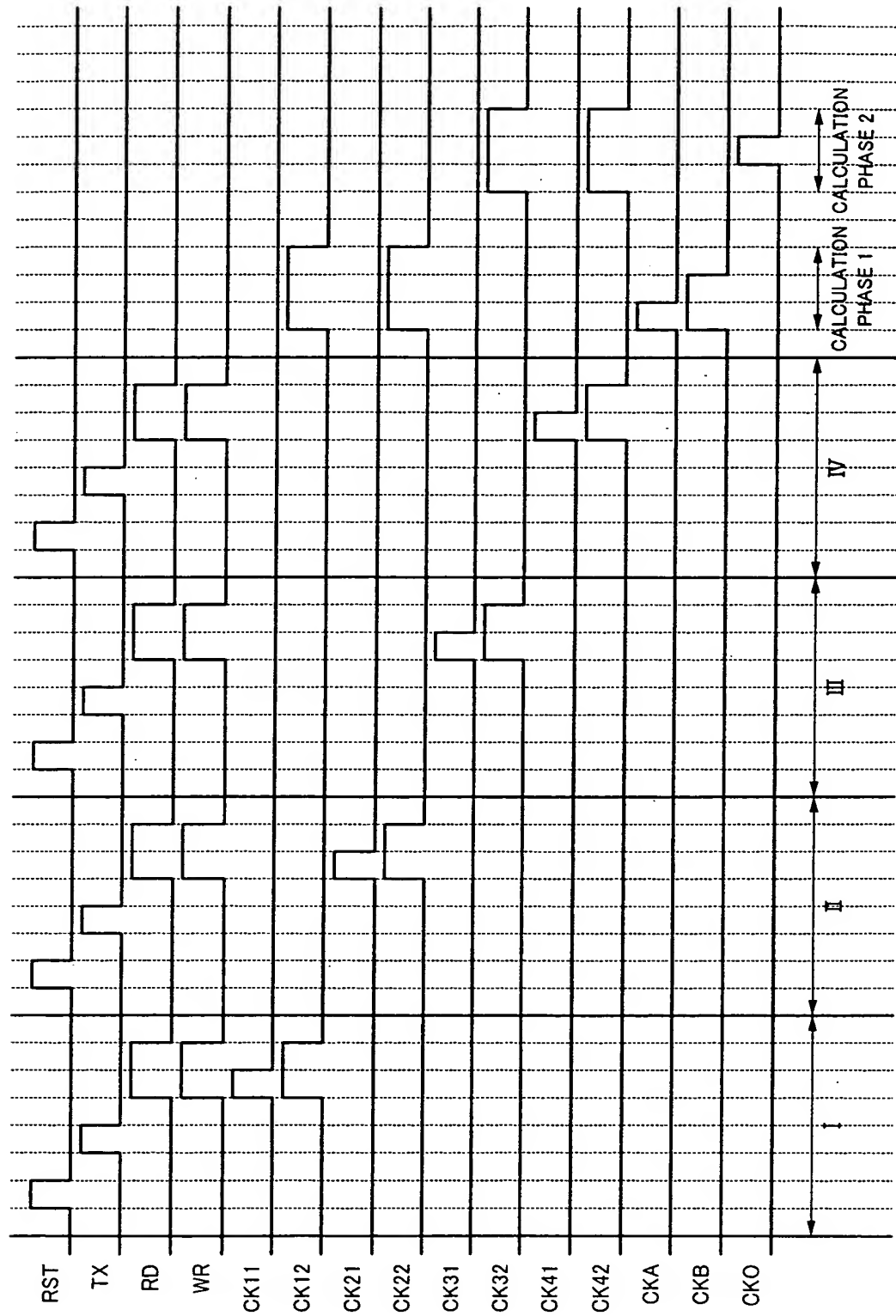
Fig. 6

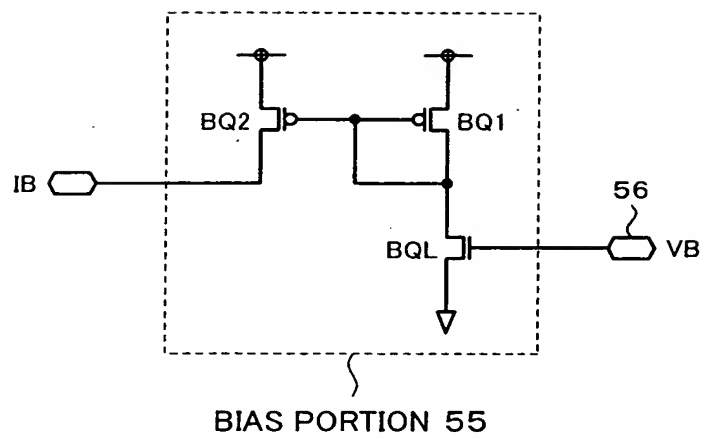
Fig. 7

Fig. 8

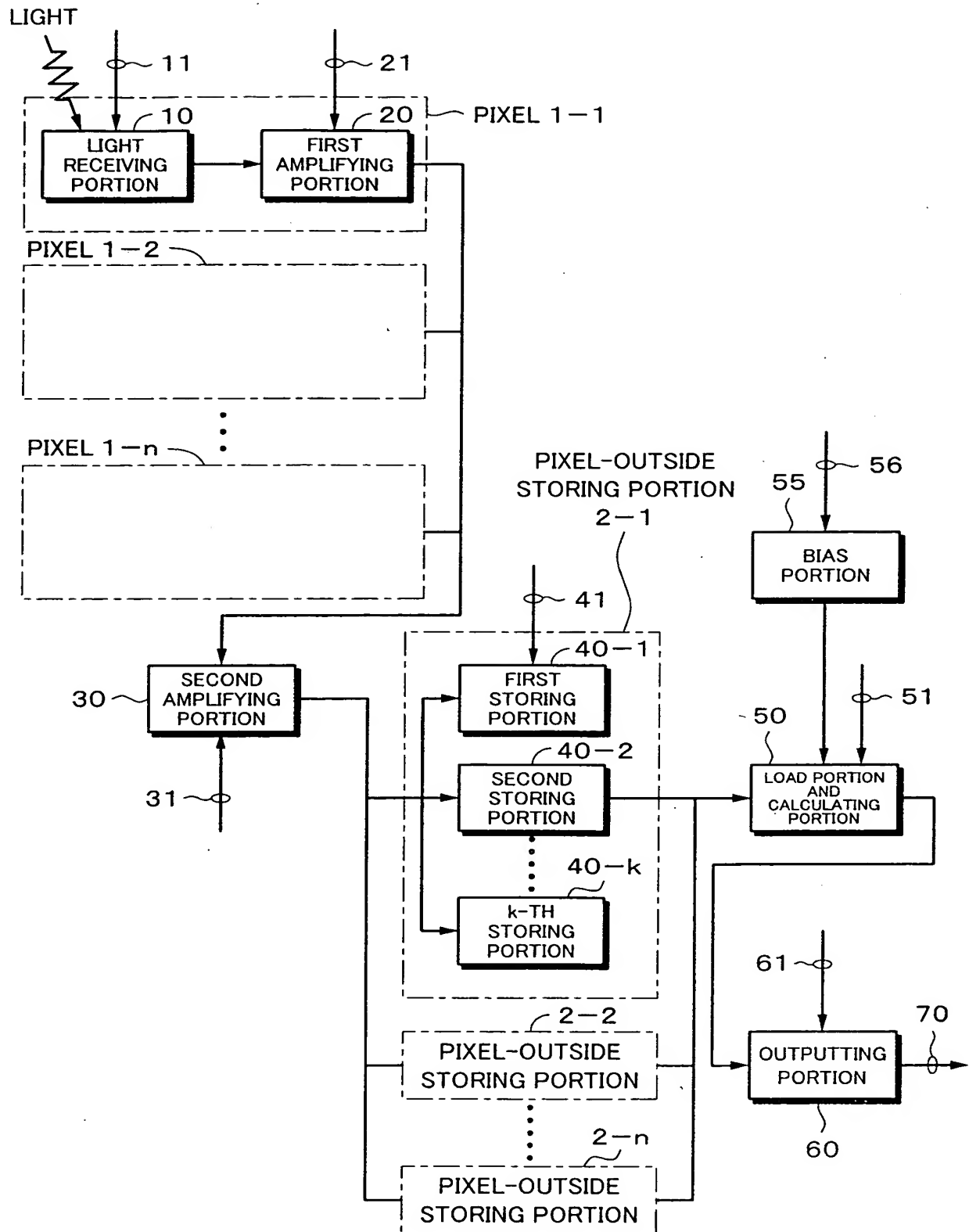


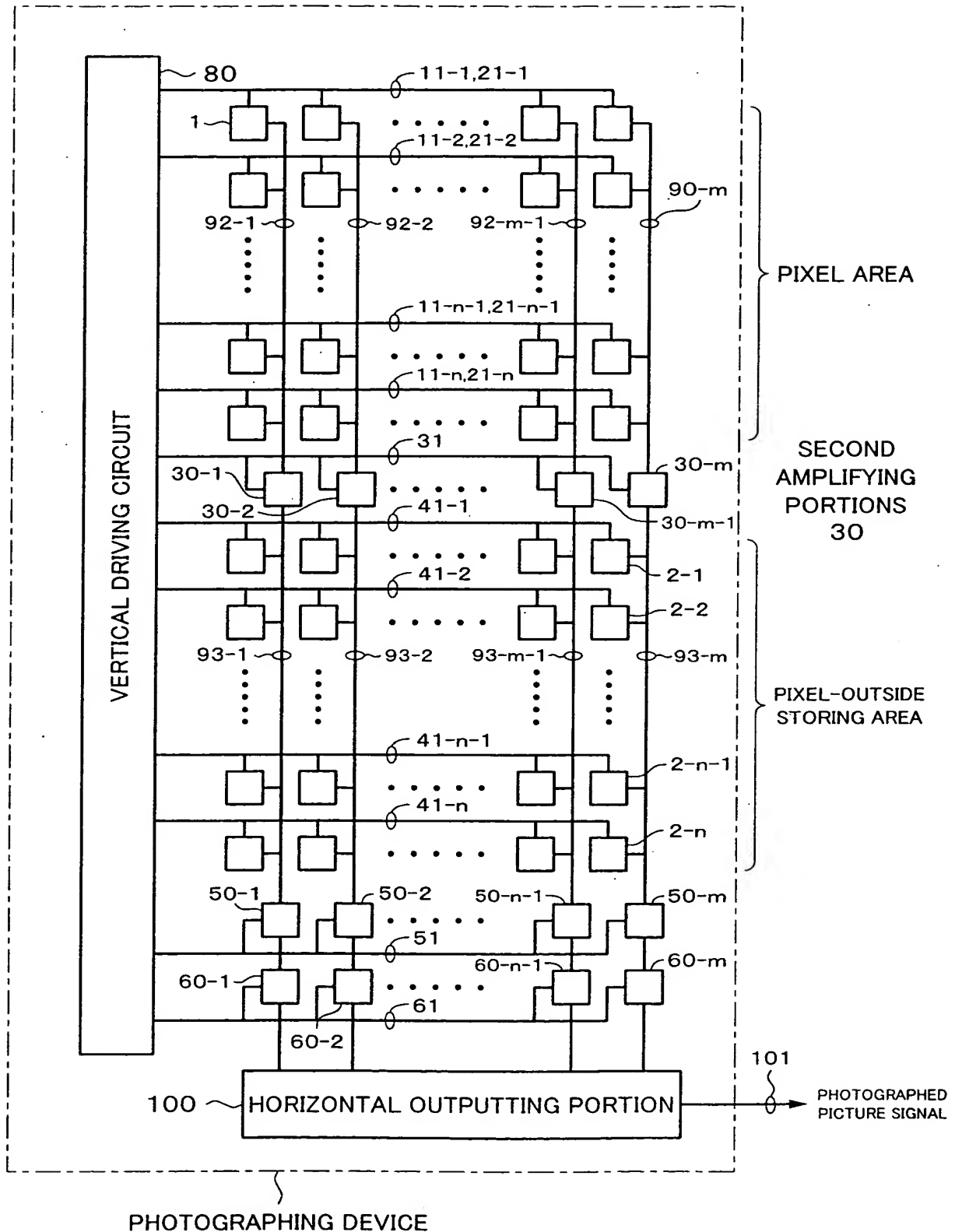
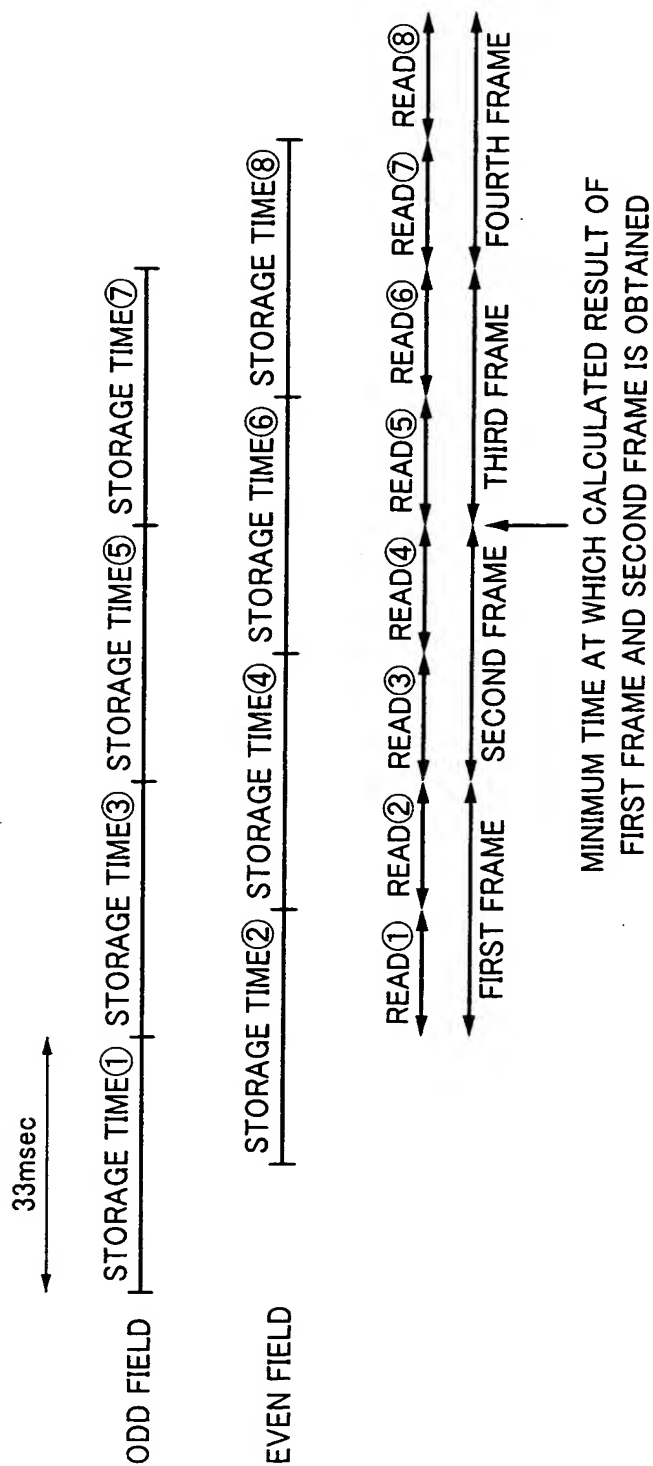
Fig. 9

Fig. 10



2050-2500

Fig. 11

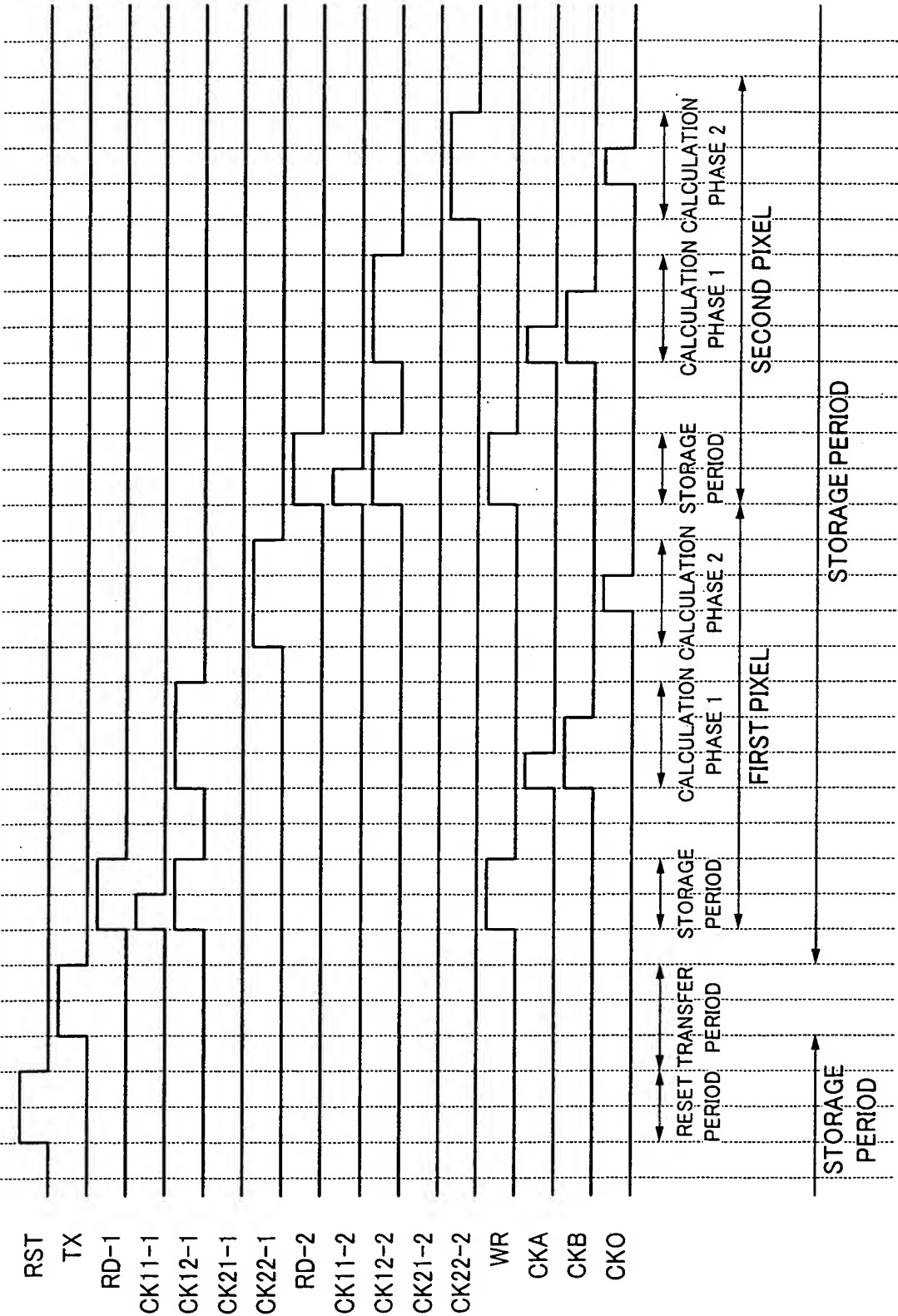


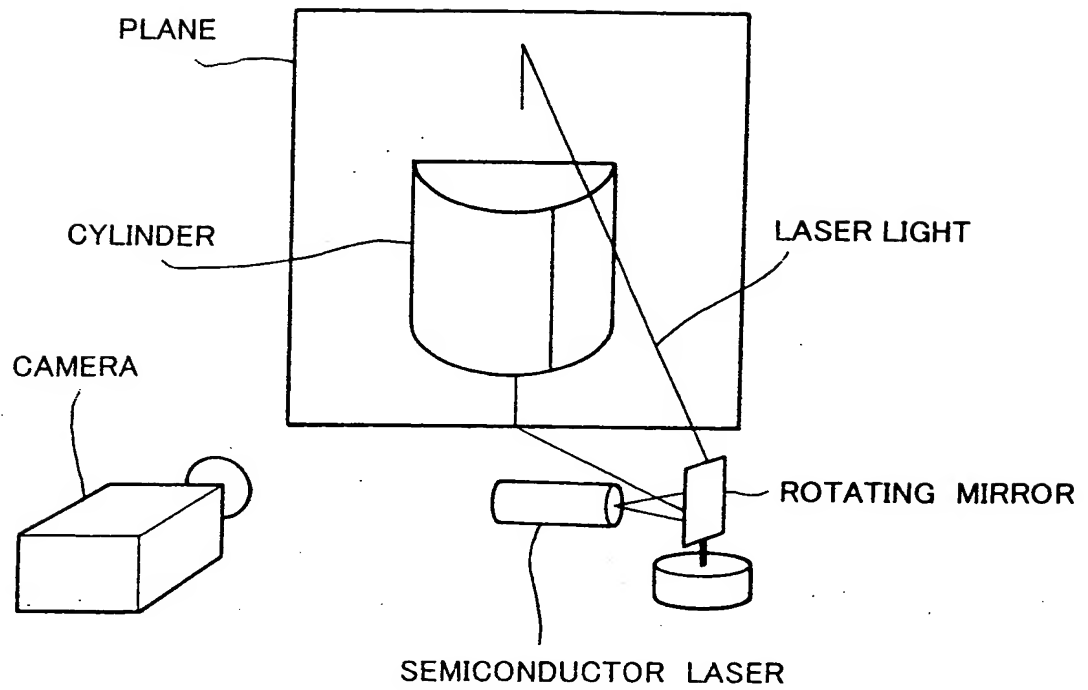
Fig. 12

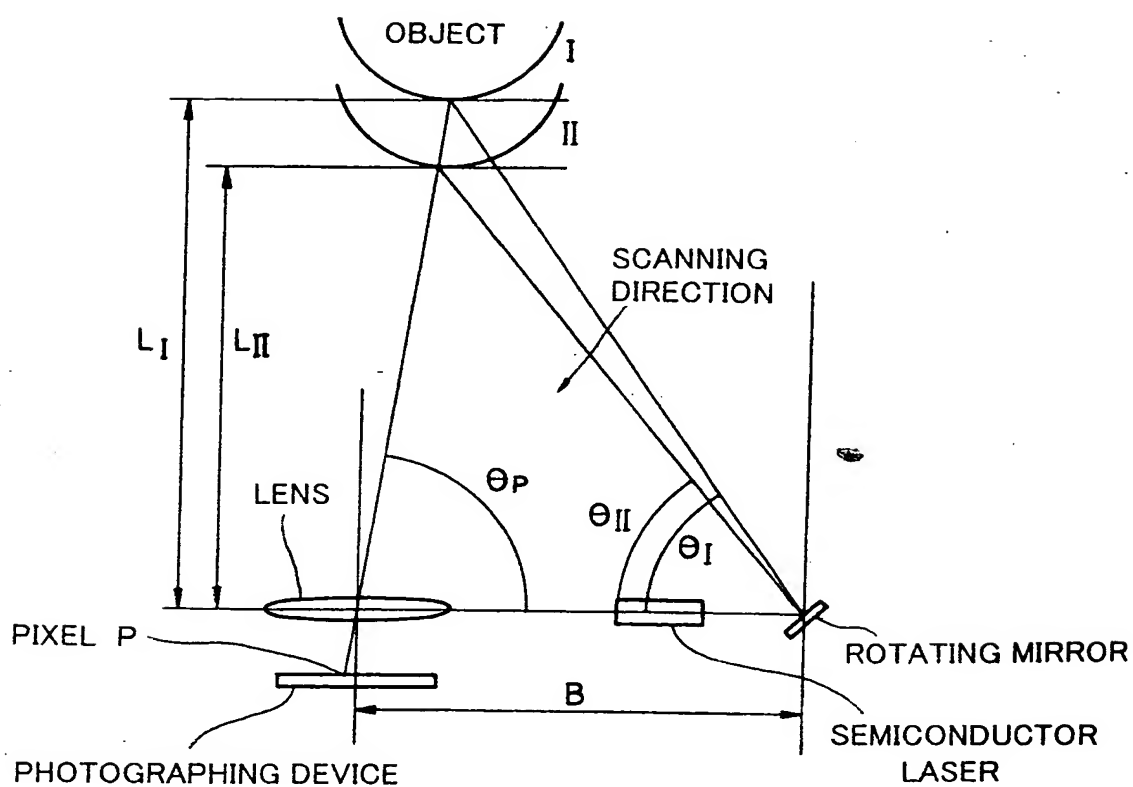
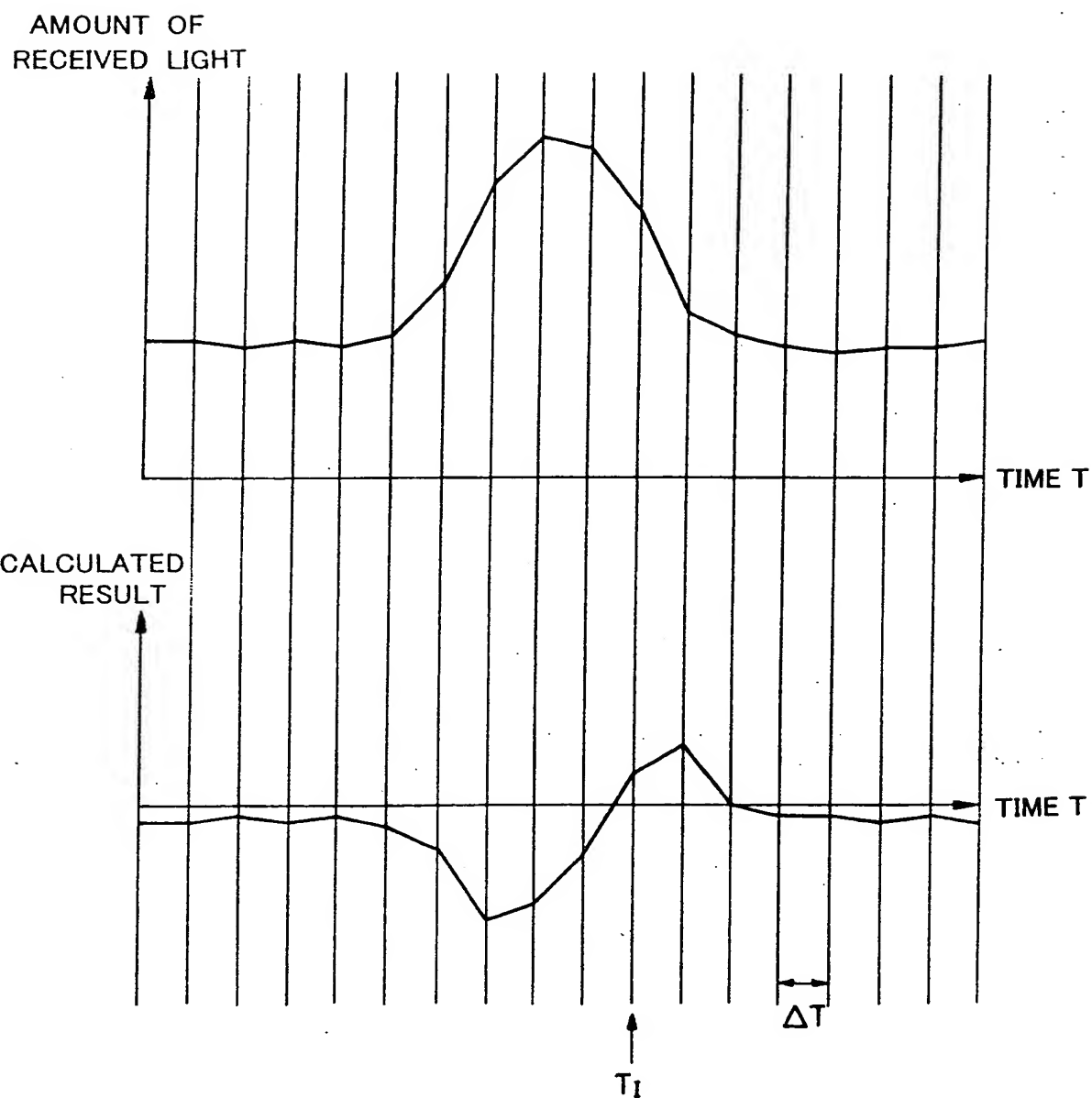
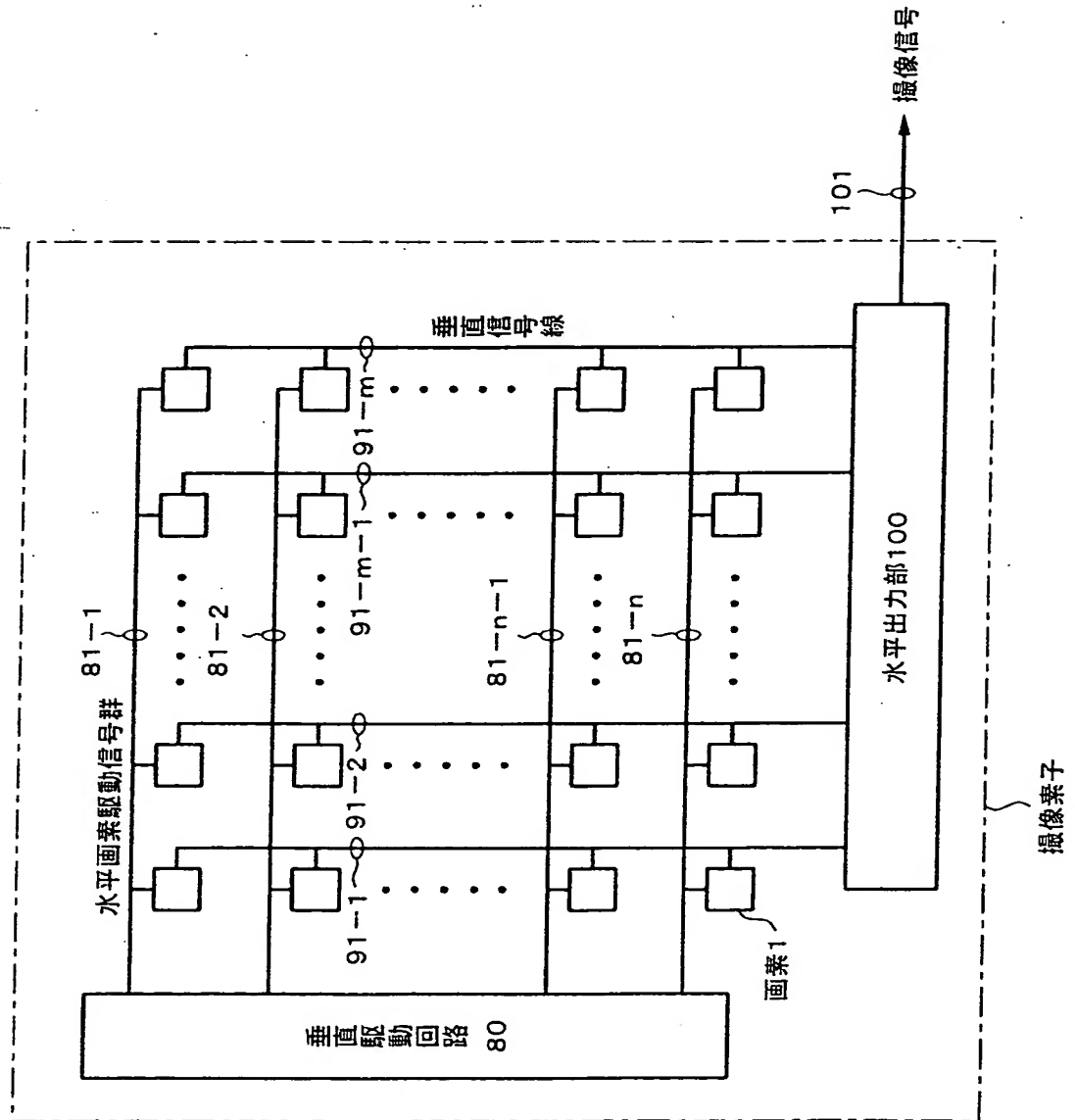
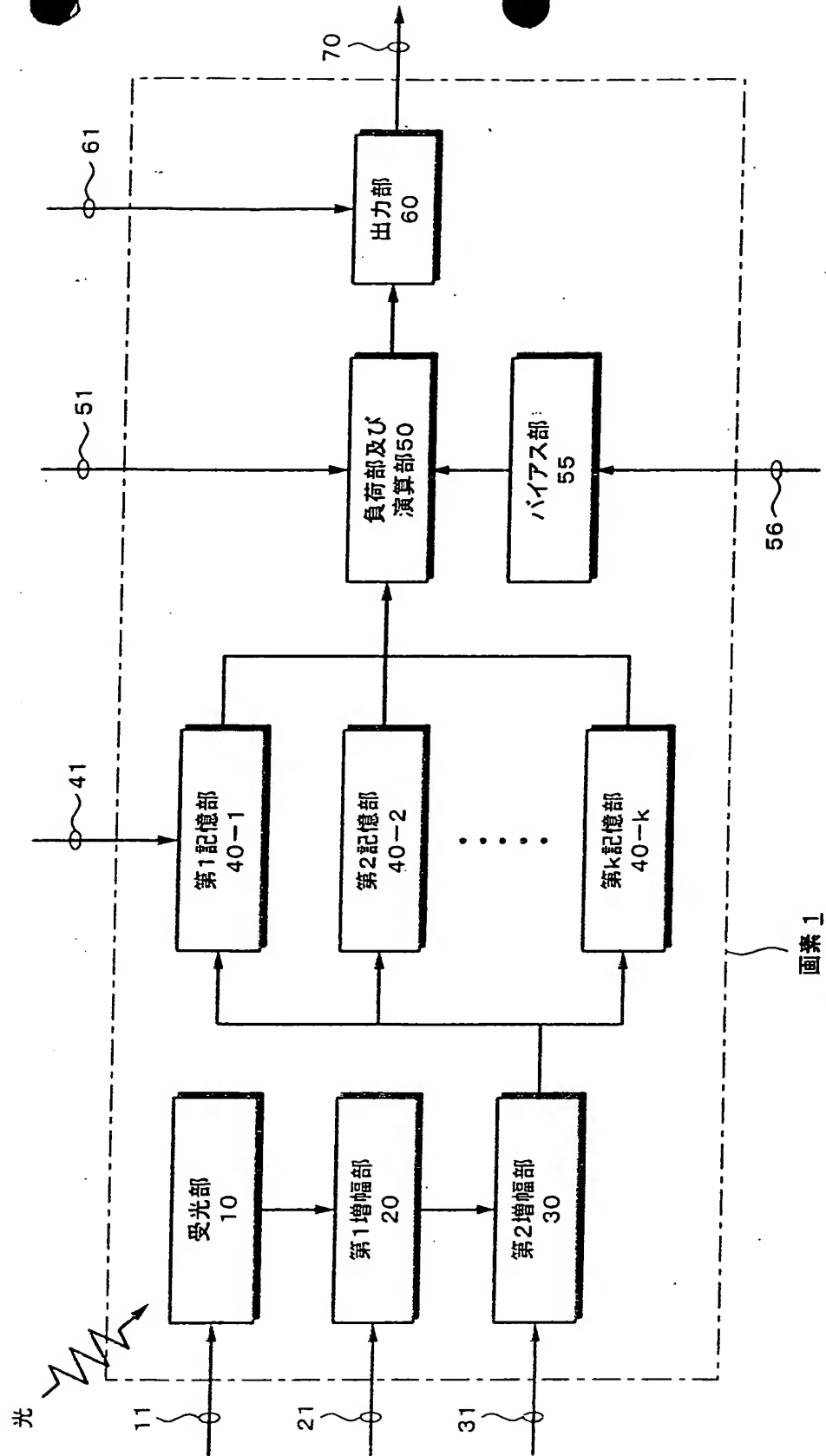
Fig. 13

Fig. 14

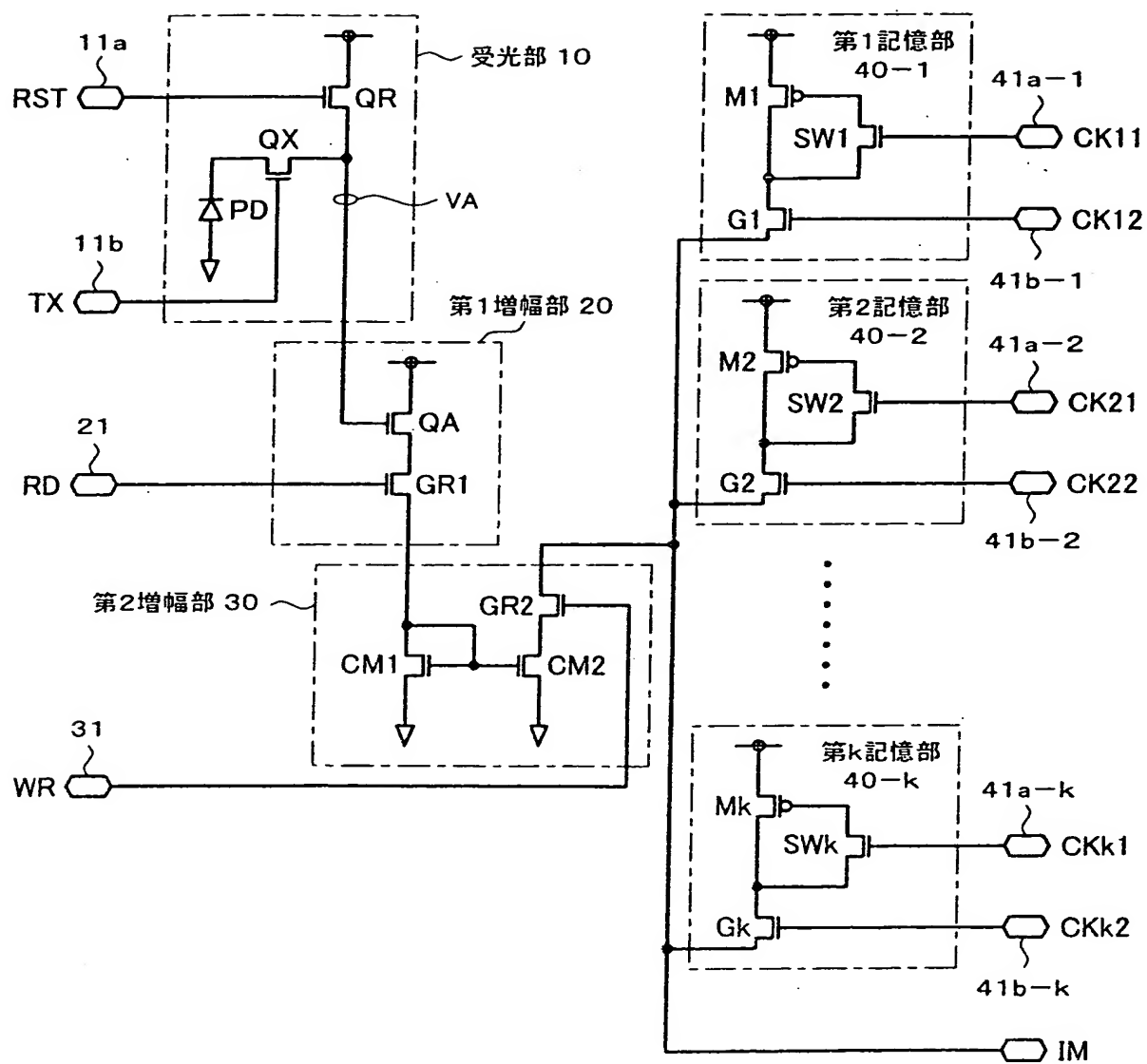
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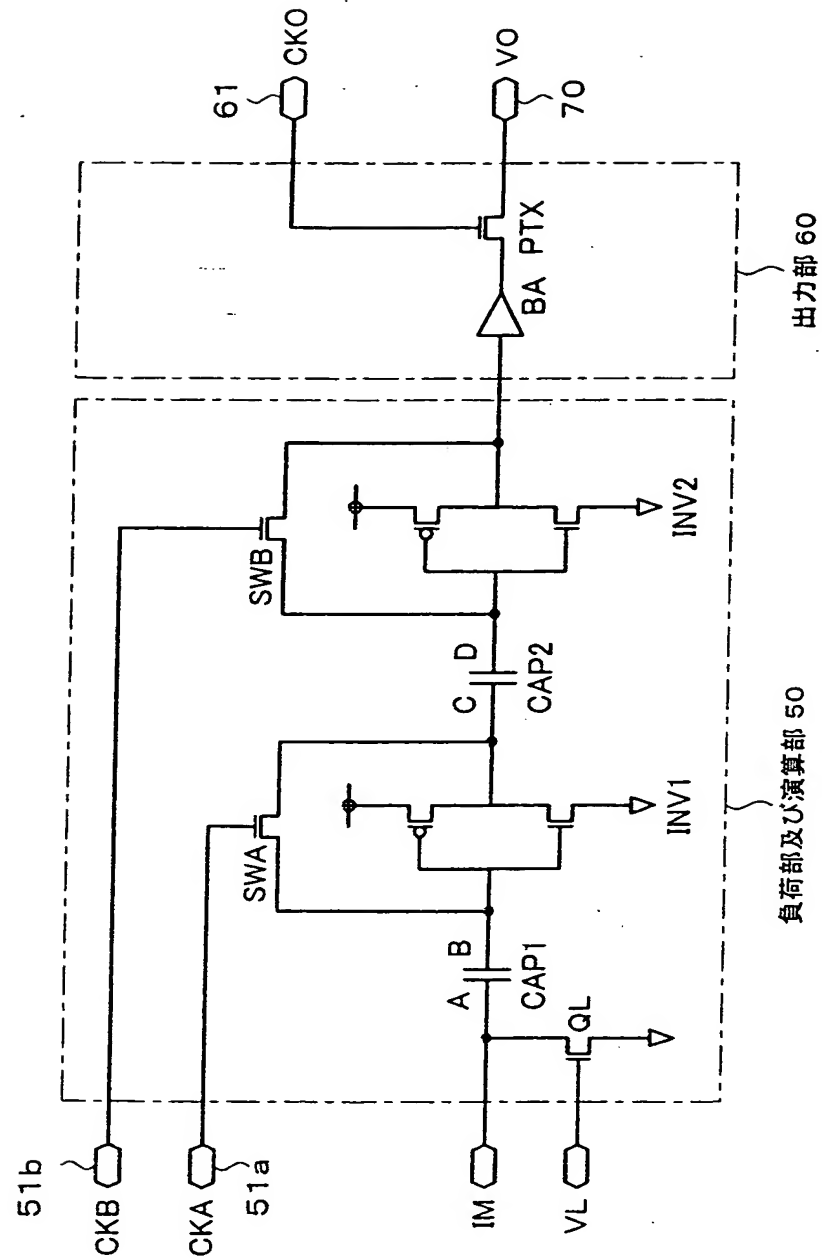
第2図



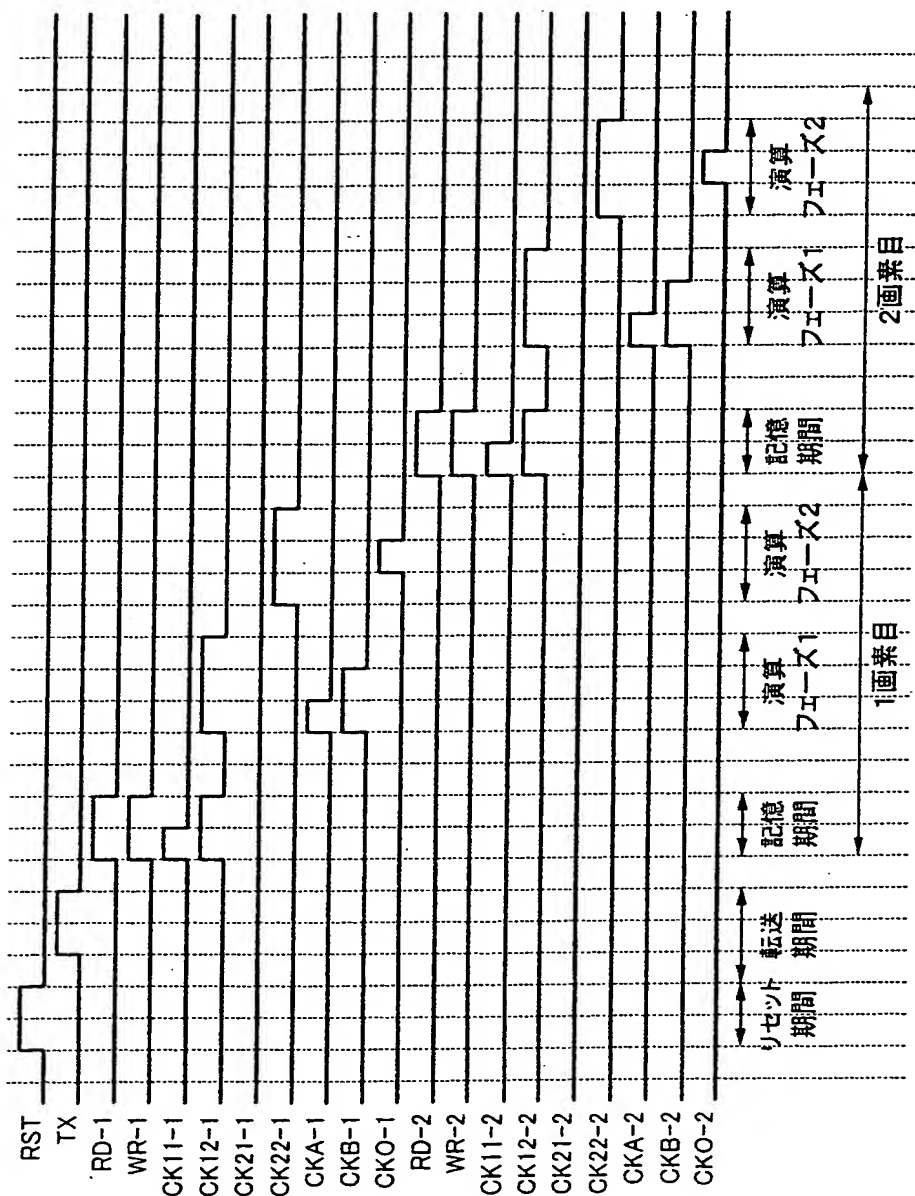
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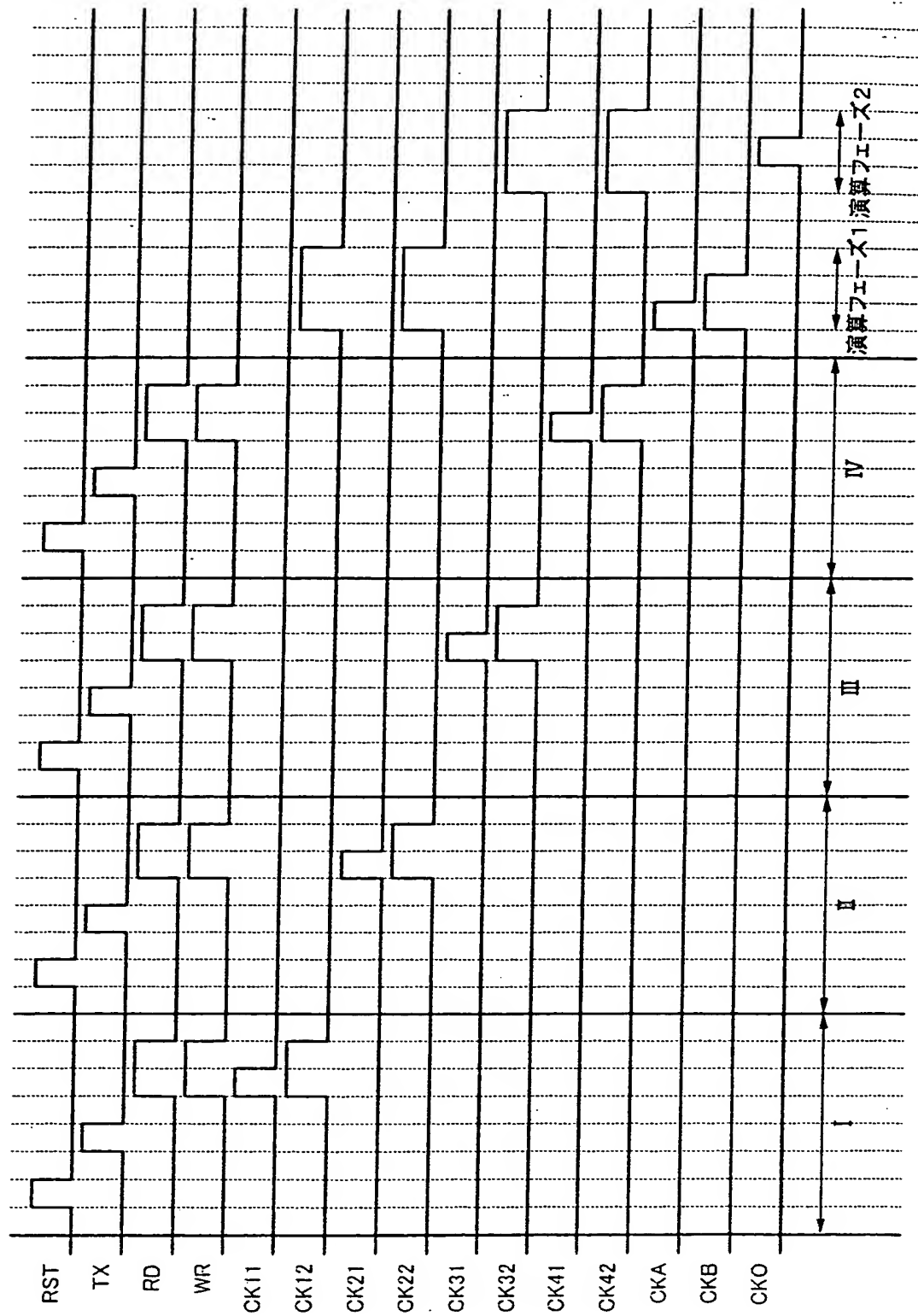
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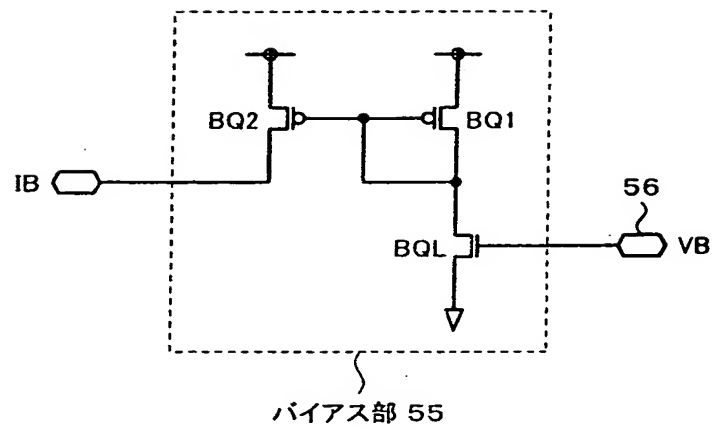
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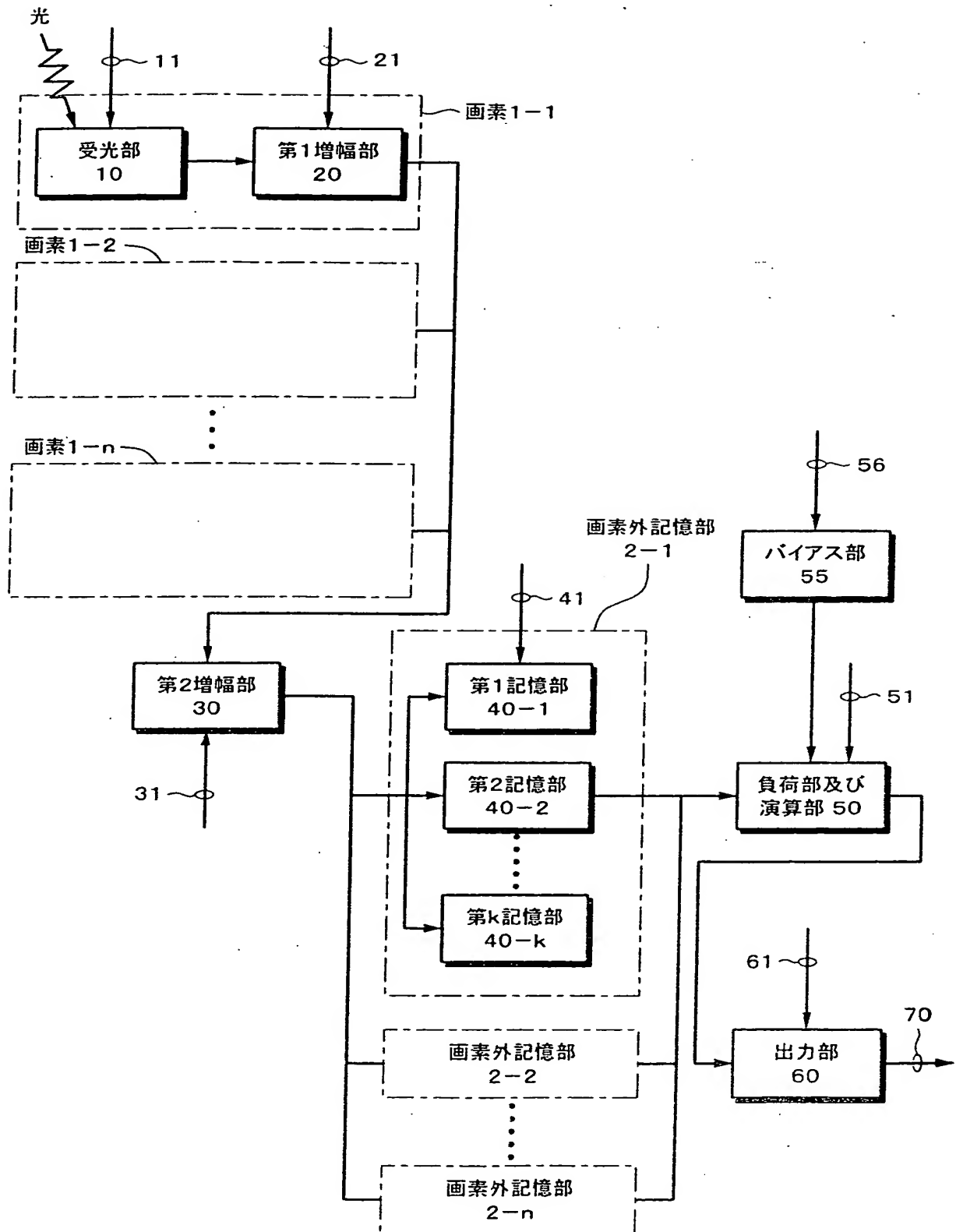
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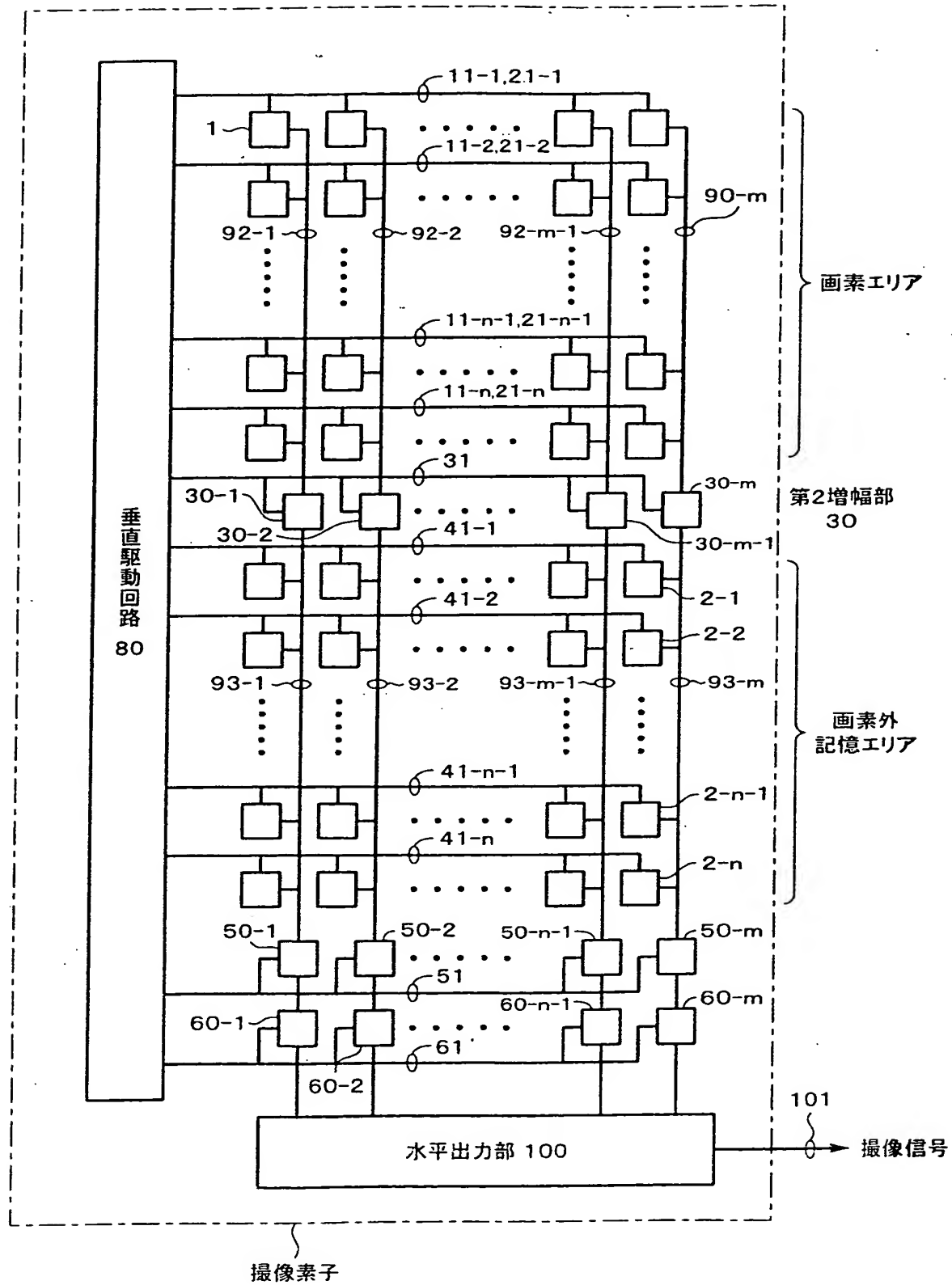
第7図



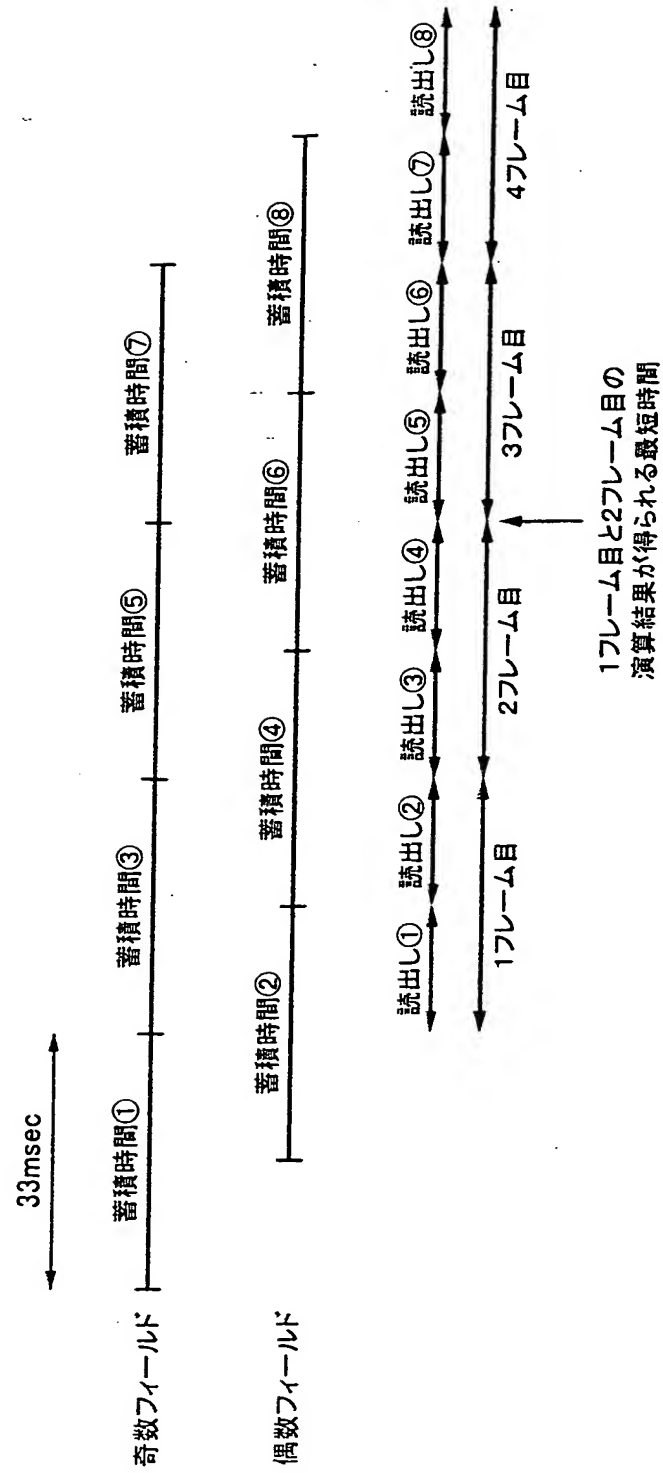
第8図



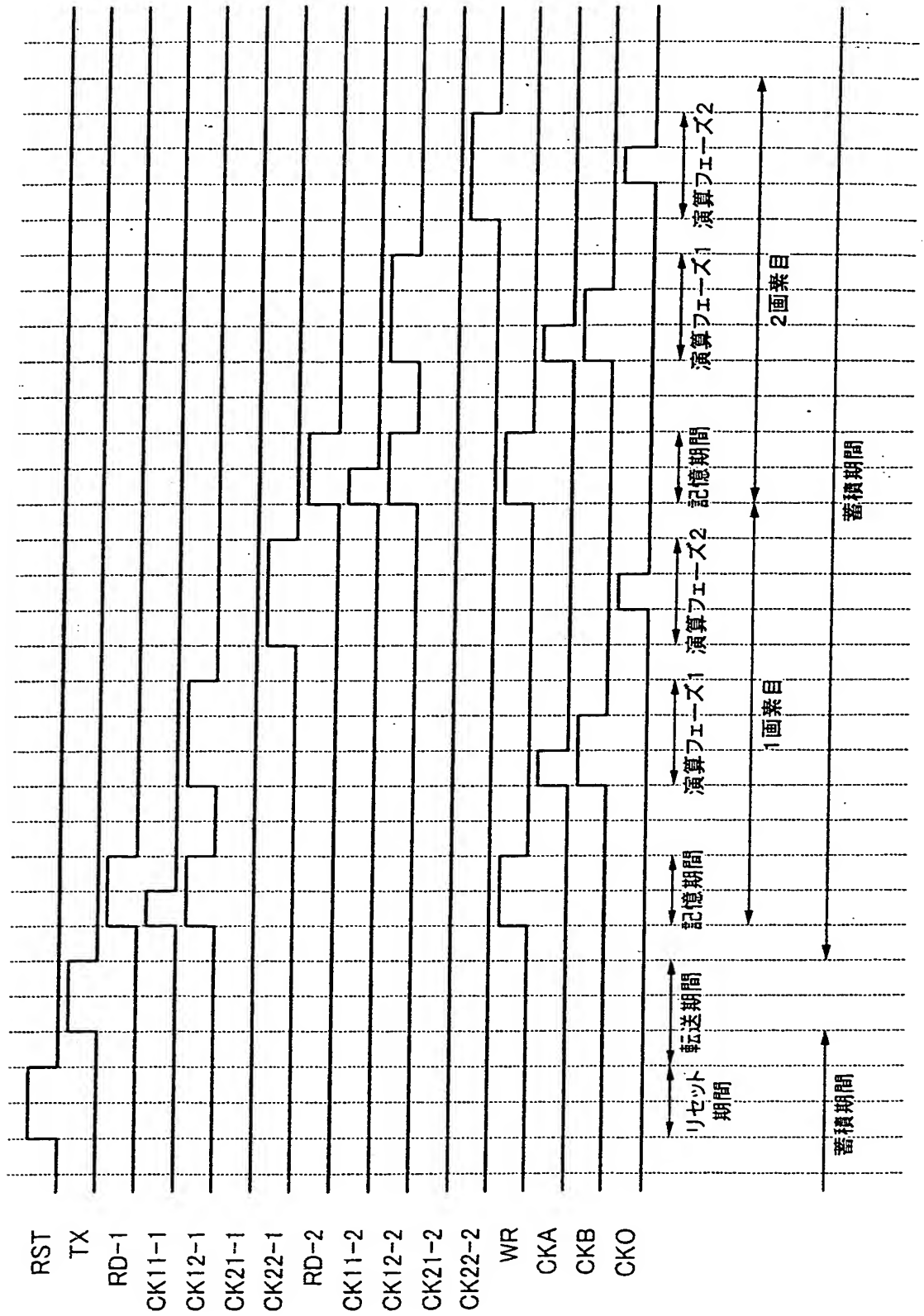
第9図



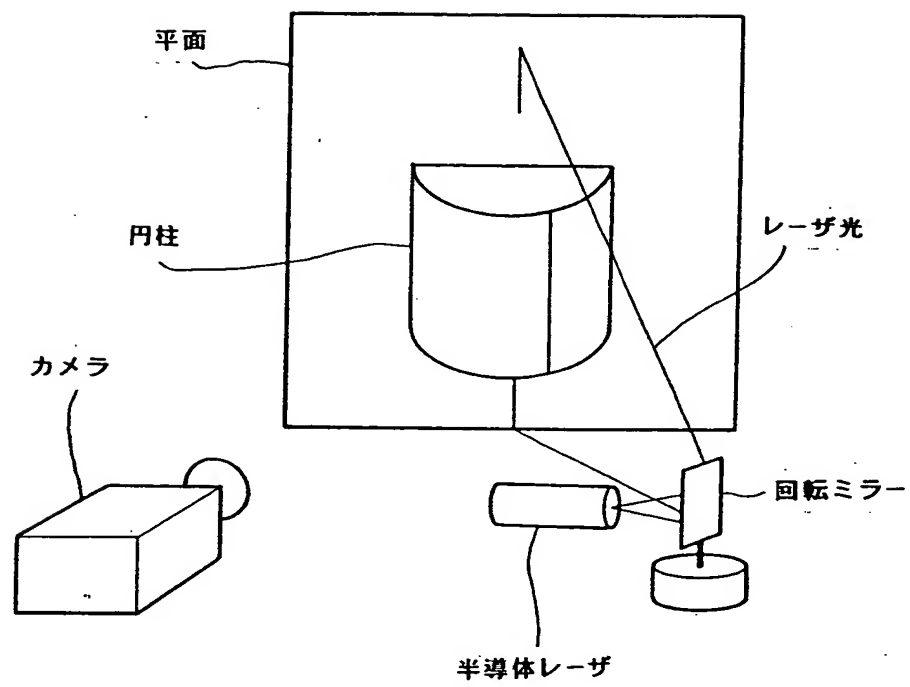
第10図



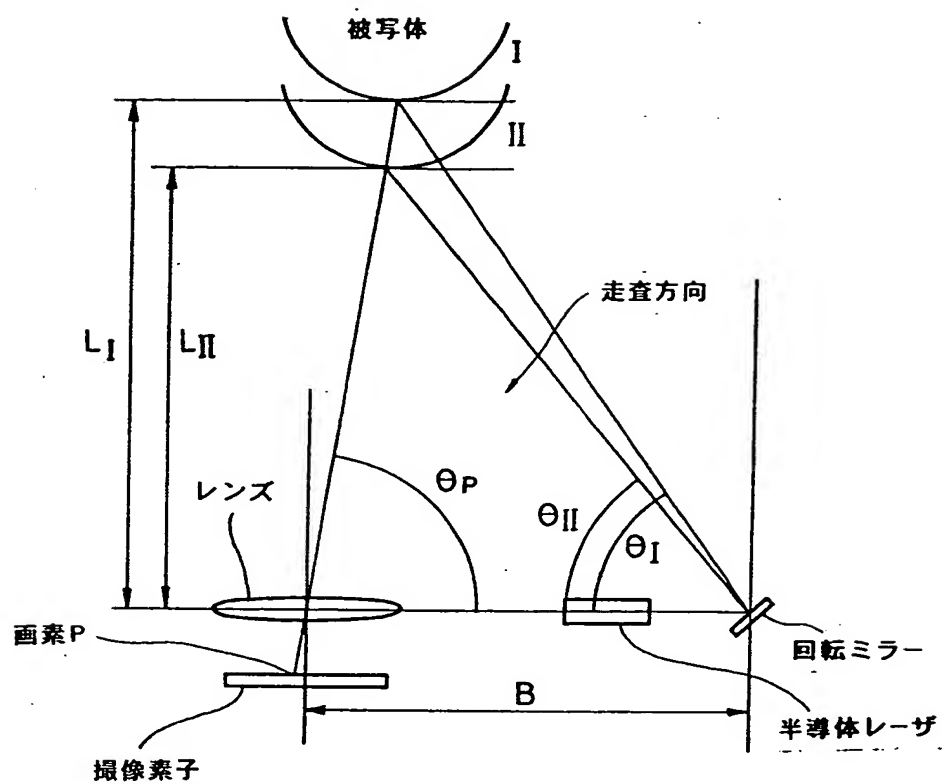
第11図



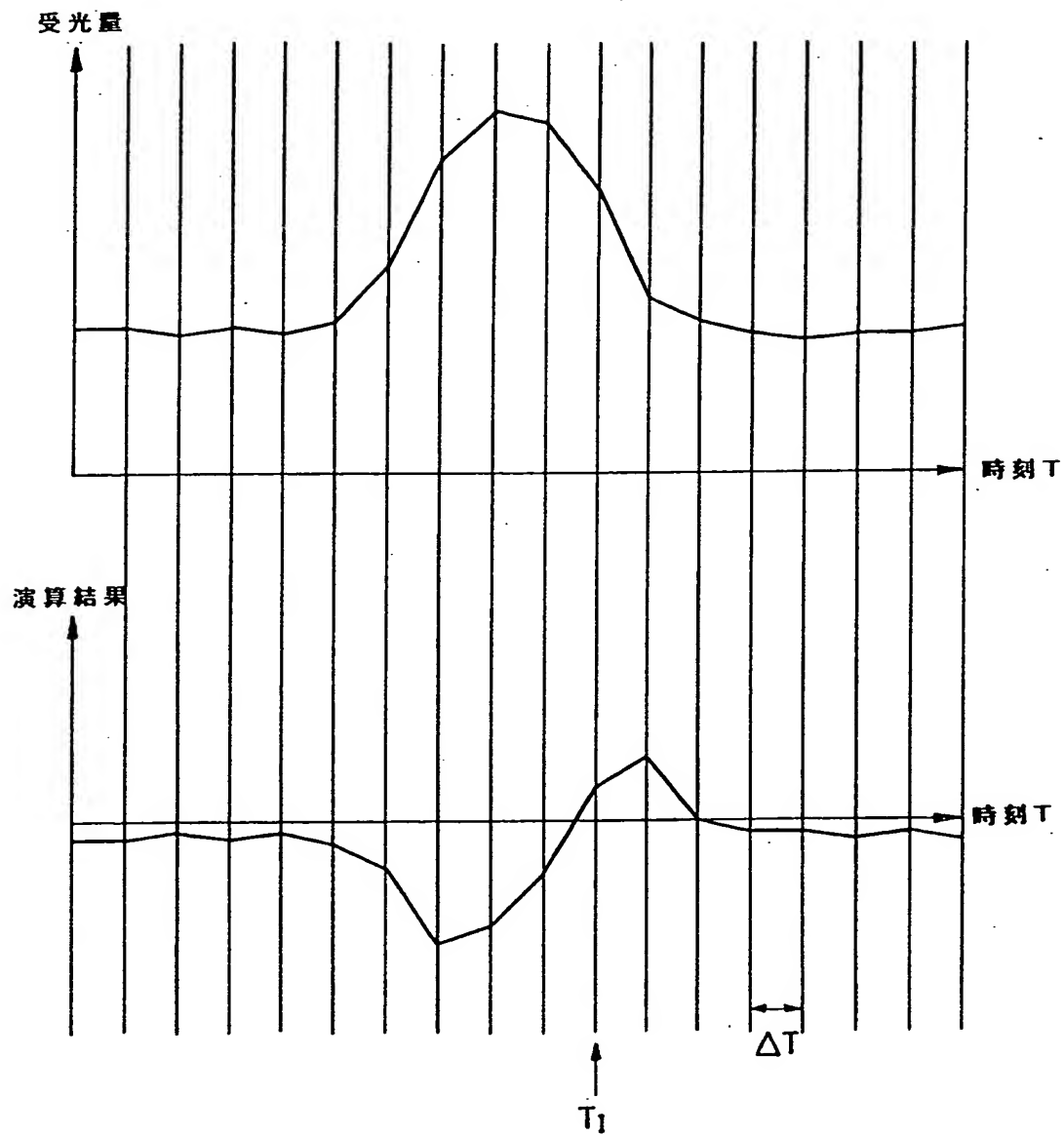
第12図



第13図



第14図



符号の説明

	1	画素
	1 0	受光部
5	2 0	第 1 増幅部
	3 0	第 2 増幅部
	4 0	記憶部
	5 0	負荷部及び演算部
	5 5	バイアス部
10	6 0	出力部
	8 0	垂直駆動回路
	1 0 0	水平出力部